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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,872	06/28/2001	Tatsuya Shimoda	109975	3054

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EXAMINER	
BAUMEISTER, BRADLEY W	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,872	SHIMODA ET AL.	
	Examiner	Art Unit	
	B. William Baumeister	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *7,11 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,12-16 and 18-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Allowable Subject Matter

1. Applicant is advised that the Notice of Allowance mailed is vacated. If the issue fee has already been paid, applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may wait until the application is either found allowable or held abandoned. If allowed, upon receipt of a new Notice of Allowance, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a specified Deposit Account.

2. Prosecution on the merits of this application is reopened on all of the claims, as the previously elected claims are considered unpatentable for the reasons indicated below:

a. The newly discovered prior art reference, Brown, provides further evidence that supports the examiner's original position and refutes Applicant's position regarding the only issue raised on appeal: whether others knew at the time of the invention that integrating ferroelectric passive matrix array memory cells and Si-based peripheral circuits was problematic because of conflicting restraints on the respective manufacturing processes.

b. The prior art references cited by the JPO and submitted in the post-allowance IDS of 9/22/04 reveal that the claims may be rejected under a broader interpretation that was not previously considered by the examiner. Specifically, the Examiner had only considered whether the claims read on prior-art fluidic-self-assembly microstructures and failed to consider whether the claims read more broadly on multichip module microstructures.

3. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Election/Restrictions

4. Initially, claims 7, 11 and 17 had been withdrawn from consideration for being directed towards non-elected inventions. These claims were rejoined upon the allowance of the elected claims because these non-elected claims either depended from or otherwise included all of the limitations of generic claims 1 and 12. However, because the allowability of these generic claims is now withdrawn, claims 7, 11 and 17 are again withdrawn from prosecution.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-6, 8-10, 12-16 and 18-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. '186, Applicant's prior art admissions and WO '170, all as applied

to the claims in the previous Office Actions, and further in view of Brown et al., Nonvolatile Semiconductor Memory Technology, 1998, pp.464-465.

i. As was explained in prior Office Actions, Applicant acknowledged in the Background section of the present application that it was known to provide "a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array" and "a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, wherein the passive matrix array is electrically connected to the peripheral circuit." More specifically, the present specification's Background section includes a discussion of WO '170, which itself, is directed towards integrating the FE-PMA with peripheral circuitry including bit-line and word-line drivers, onto a common substrate. In the present specification's Background section, Applicant (1) acknowledges that WO '170 constitutes prior art; (2) acknowledges that WO '170 is directed towards ferroelectric passive matrix array (FE-PMA) (see e.g., FIGs 24-26 of the present application); and (3) further describes manufacturing problems associated with integrating the type of prior-art FE-PMA/peripheral circuit memory device that is taught by WO '170. Applicant's patent application is directed towards a solution to this problem.

ii. As stated, the problem discussed in Applicant's Background section relates to the integration of the FE-PMA and the Si-based peripheral circuits. Specifically, the process temperatures required for forming the two respective structures differ greatly. So when both structures are formed on a common substrate, the quality of at least one of these

structures is negatively affected. Applicant's solution to this problem was to form the FE-PMA memory portion, the peripheral Si-based circuit portion, or both on a separate "microstructure" or respective microstructures and then integrate the microstructure(s) onto a common substrate.

iii. The integration of separately-formed microstructures onto a substrate, both in concept and as claimed, reads on the fluidic-self-assembly process of Smith et al. '186. Specifically, Smith discloses that whenever problems in manufacturing or the like interfere with the integration of dissimilar electronic components, some or all of the components can be separately formed on microstructures, and the microstructures then integrated onto a common substrate by a fluidic-self-assembly (FSA) process.

iv. Accordingly, the examiner previously took the position that combining Smith's general teachings of the FSA process with the specific teachings relating to FE-PMA circuit integration, as set forth by Applicant's discussion of prior-art WO' 170 and/or WO '170, itself), would render obvious the structures presently claimed. The motivation to combine these teachings included the facts that (1) WO '170 and applicant's admissions each teach that the desire to integrate FE-PMAs with peripheral circuits was known, (2) Applicant had acknowledged that the manufacturing problems associated with actually doing so were known, and (3) that Smith provided a solution to this conventionally-known problem. The Examiner's position and explanations are more fully set forth in prior Office Actions. The non-final rejection of 8/19/03 might be deemed to be the single best example of the Examiner's position regarding all of the claims.

v. On appeal, Applicant did not dispute most of the foregoing facts, positions, and bases set forth by the examiner. For example, Applicant did not dispute that combining the cited prior-art references would produce structures that read on the claims. Rather, Applicant only raised one single issue on appeal. Applicant only argued that his discussion of the admitted prior art in the Background section of the present application did not include a specific admission that the problem of integrating the various prior-art components was recognized; but rather, that it was Applicant who recognized that a problem resulted from integrating FE-PMAs with Si-based circuitry. Applicant therefore urged (1) that since he did not admit that others knew of the integration problem, the Examiner's reliance on the existence of this integration problem as the motivation to combine the prior-art references was improper, and (2) that the Examiner had therefore failed to establish a *prima facie* case of obviousness. The examiner's sole reason for subsequently withdrawing the rejection and allowing the claims was based on Applicant's assertion that the problems with integration were discovered by Applicant and not previously known by the public.

vi. The newly discovered Brown reference unequivocally refutes Applicant's position on this issue. Brown states, "[r]ecently, ferroelectric memories have appeared as candidates for radiation-hard nonvolatile memories. The basic cell [would be promising], but so far the problems of integrating their manufacture with the process for silicon ICs has not been completely solved." Restated, regardless of whether Applicant may have independently discovered the existence of problems relating to the integration of ferroelectric and Si-based structures, Brown supports the examiner's original position

that prior to the invention, others were also aware of this integration problem. As such, the examiner's motivation to combine was proper; the examiner did, in fact, establish a *prima facie* case of obviousness; and the burden has shifted to Applicant to rebut the examiner's showing of obviousness.

vii. Applicant has not provided any evidence that others were unaware of this integration problem. In fact, Applicant has never even argued that others were unaware of this integration problem. Applicant's representative has only argued (for the first time on appeal) that Applicant had not admitted the fact that others knew of the integration problem. Moreover, Applicant has raised no other arguments on appeal. As such, Applicant has not provided any argument or evidence whatsoever that would rebut the Examiner's *prima facie* showing of obviousness. The rejections are therefore proper.

7. Claims 1-4, 8-10, 12-14, 19, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art admissions and WO '170 and Brown, all as applied to the claims above, and further in view of JP 8-167,703.

a. As was explained hereinabove, Brown in combination with Applicant's prior art admissions and/or WO '170 teach that driving FE-PMA memories with Si-based peripheral circuits was known (e.g., Brown and WO '170); the desire to integrate the memory and driver onto a common substrate was known; it was known that the differing processing requirements made this historically difficult (e.g., Brown); WO '170 attempted to overcome this by balancing the processing conditions and therefore balancing the negative impact on either of the two structures. None of Applicant,

WO'170 or Brown discloses integrating on a common substrate, FE-PMAs and Si-based peripheral circuits wherein at least one has first been separately-manufactured on a microstructure.

b. JP '703 teaches that multi-chip module (MCM) technology may be employed, whereby separate separate circuits or electronic components are formed on separate chips (or "microstructures") and then integrated onto a common substrate. See e.g., claims 1, 2, and 7 stating that memory and memory peripheral circuits may be formed on separate chips. Also see e.g., paragraphs [0080] – [0082] and FIGs 11 and 12 wherein plural, centrally-located memory chips 121 and separately-formed memory peripheral circuit chip section 122 are mounted on substrate 120.

c. It would have been obvious to one of ordinary skill in the art at the time of the invention constructing a device including conventional FE-PMAs and Si-based peripheral circuits as taught by Applicant/WO '170/Brown to have manufactured them in separate chips and integrated them on a common substrate through an MCM process as taught by JP '703. The ordinarily skilled artisan would have been motivated to do so for the purpose of achieving increased integration (a goal taught by WO '170 and JP '703) while simultaneously obviating the need for compromising the quality of either device, as was required for forming integrated structures according to WO '170.

d. Claim 1, e.g., sets forth that the peripheral circuit is formed on the substrate, and claim 2, e.g., sets forth that the FE-PMA is formed on the substrate. The language for both of the claims is broad enough to read on structures wherein the cited component is either (1) formed directly on/in the surface of the substrate, or alternatively (2) formed

on/in a separate microstructure (or chip) that is, in turn, mounted on the substrate by conventional MCM techniques, similar to claim 3.

e. Regarding the claim language further setting forth "an associated circuit having a same or a different function as the memory cells" (e.g., claim 8), this language reads on an additional FE-PMA cell/circuit, and is rejected under the same theory as are plural FE-PMAs, as set forth above.

f. Regarding claims 10 and 18, further setting forth that peripheral microstructure is larger than the FE-PMA microstructure, the particular size of each ultimately chosen will depend upon conventional considerations such as how much memory is desired for a particular application and how many other Si-based circuits are desired to be integrated with the Si-based peripheral circuits. As such, the provision of the respectively sized chips does not produce any novel or unexpected results.

8. Claims 5, 6, 15, 21 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art admissions; WO '170; Brown and JP '703 ("the base references") as applied to the claims above and further in view of JP 5-275,611.

a. The base references teach the FE-PMAs and Si-based peripheral circuits that are integrated using an MCM technology as explained above. Regardless of whether JP '703 discloses as much, JP '611 teaches that a substrate on which MCM chips are supported may be provided with recessed portions that correspond to the shape of the MCM chips or "microstructures." It would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the substrates of such MCM devices formed

according to the base references with such recesses for the purposes of enabling wiring lengths to be decreased and device speeds to be increased as taught by JP '611.

b. Regarding claim 6, the product-by-process doctrine applies, and the burden is on applicant to show that the recited process necessarily results in some structural difference.

Response to Arguments

9. Applicant's arguments filed in the Appeal Brief have been fully considered but they are either not persuasive for the reasons set forth previously and hereinabove in relation to the narrow interpretation, or are moot in light of the new grounds of rejection based upon the broader interpretation.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Messenger et al., "FERROELECTRIC MEMORIES: A POSSIBLE ANSWER TO THE HARDENED NONVOLATILE QUESTION," IEEE Transactions on Nuclear Sciences, Vol. 35, No. 6, December 1988, pp. 1461-1466. This article was cited by the Brown reference discussed hereinabove.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to B. William Baumeister whose telephone number is (571) 272-1722. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRADLEY BAUMEISTER
PRIMARY EXAMINER

B. William Baumeister
Primary Examiner
Art Unit 2815

December 15, 2004